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Efficient Design Techniques of Flash ADC for High Speed and Ultra Low Power Applications

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ABSTRACT

Analog to Digital converters are the essential components of todays digital world. As these convert real time signal into its equivalent digital code, must be designed efficiently. This paper presents design of 3-bit high speed and power efficient Flash Analog to Digital Converter. Flash type Analog to Digital Converter is designed and implemented with different inverter based comparators and based ROM encoder. A high speed ROM encoder is designed to convert thermometer code to its equivalent binary code. The proposed research compares various inverter based comparators such as Threshold Inverter, Quantizer comparator, Single Inverter Comparator, Single Inverter Comparator with the reference voltage and LTE comparators, designed using cadence design tools with 180nm technological library. The simulation results show that Single Inverter Comparator consumes less power 5.647uW among TIQ and R-TIQ comparators. Single Inverter comparator with reference voltage consumes less power however with more delay. Here Flash ADCs are designed with various inverter based comparators and ROM encoder. The results show that TIQ comparator based ADCs consume power of 298.9uW, whereas ADC designed with Single Inverter Comparator consumes 459.8uW power.

KEY WORDS: ITIQ COMPARATOR, ROM ENCODER, SINGLE INVERTER COMPARATOR, TIQ COMPARATOR.

INTRODUCTION

Analog to digital converters are the critical components of digital communication system. Flash ADC is suitable for applications requiring very large bandwidths due to its high speed. But power consumption is more because of an array of comparators to achieve parallel operation. It is used in digital oscilloscopes, radar, high density disk drives, IoT applications and in communication systems. The power consumption of the Flash Analog to Digital converter has to be reduced in order to have efficient communication system. The three main design parameters of ADCs are speed, power consumption and area. To achieve high speed and lower power consumption, ADCs are implemented in variety of architectures.

The Flash architecture enables lower latency, superior flexibility and lower metastability error rate than other high-speed, low-to medium resolution ADCs. Block diagram of the Flash ADC is depicted in Fig. 1 (Lavania, Y et al., 2013). The three major components of Flash ADC are resistor ladder, comparator and an encoder. A resistor ladder generates reference voltages by voltage divider network. Each comparator compares the applied input voltage with reference voltages; if the applied input voltage is greater than reference voltage, comparator gives '1' as its output, otherwise '0'. An encoder converts thermometer code to an equivalent digital code.

A Threshold Inverter Quantizer comparator proposed in (Yoo, J. et al., 2003), proposed that "the reference voltages are generated by varying the length and width of the

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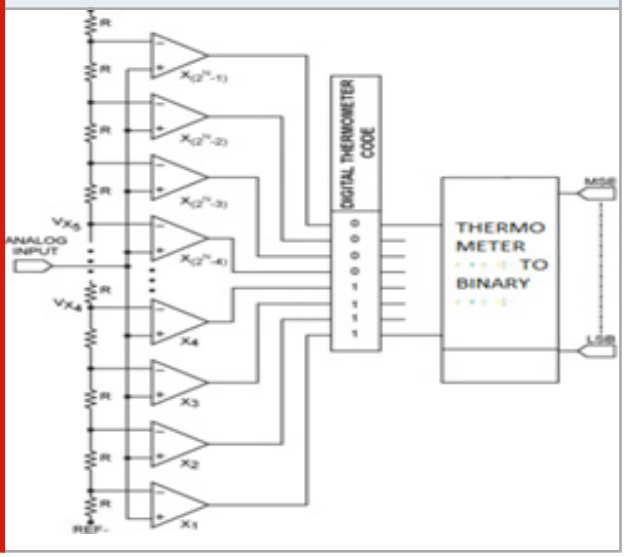
transistors as threshold voltage is the function width 'W' and length 'L'. TIQ comparator has two inverter circuits cascaded. The first one does comparing and the second balances. This circuit replaces the resistive ladder which consumes more area and results into more static power dissipation. The TIQ comparator is one of the high speed, area and power efficient techniques for designing Flash ADCs. The Linear Tunable Transconductance Element introduced in (Kulkarni, M. et al., 2010) reduces the power consumption by connecting two more transistors on either ends of the inverter circuit.

Figure 1: Block diagram of Flash Analog to Digital Converter

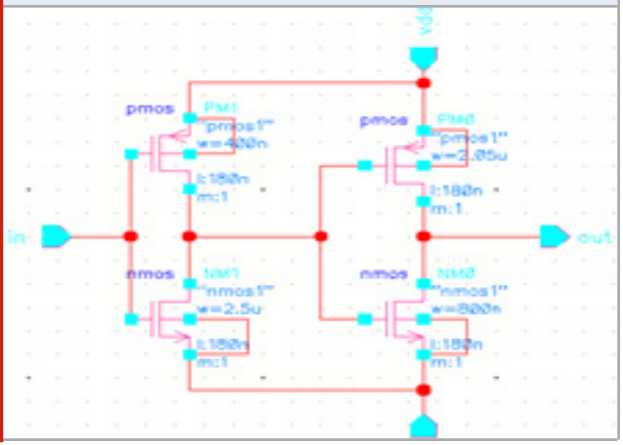


It shows a good improvement in power supply rejection ratio of the design but operates over the very little portion of the input signal swing. In (Gupta, Y. et al., 2014; Hosur, K.N. et al., 2015; Kar A. et al., 2015; Perumal, I. et al. 2009) proposed that Threshold Modified Comparator circuit operates over good range of input signal swing by varying 'W' and 'L' of TIQ comparator over a wide range, hence occupies more area. To enhance the range of signal swing Single Inverter Comparator with reference voltage is proposed in (Kalyani, N. et al., 2018). An improved TIQ comparator ITIQ with extra two pMOS transistors is proposed in (Prathiba, G. et al., 2018). A 3-bit Flash ADC is designed and analyzed with different inverter based comparators as they are power and area efficient circuits with high speed. The FADC design has seven comparators and 7:3 ROM based encoder. The paper compares performance of different inverter comparators and performance of FADC with each these comparators and ROM encoder.

Design of Comparators: The design of comparator is the most important part of the Flash ADC as the number of comparators doubles with 1-bit increase in the resolution of ADC. Power consumption of these comparators can be reduced by using different design techniques. This paper compares different parameters of Threshold Inverter Quantizer (Yoo, J. et al, 2003; Perumal, I. et al., 2009) Linear Tunable Transconductance Comparator (Kulkarni, M. et al., 2010) and Single Inverter Comparators (Kalyani N. et al. 2018) and ITIQ proposed in (Prathiba, G. et al., 2018).

TIQ Comparator: TIQ Comparator has two inverters connected in series for comparing and balancing. By varying 'Wn' and 'Wp' of the transistors the threshold voltage of the inverter circuits are changed to obtain different reference voltages. The Fig. 2 shows the designed TIQ comparator circuit which operates over 0.59V to 0.930V of input signal swing.

Figure 2: Threshold Inverter Quantizer Comparator



Equation 1 is used to obtain different threshold voltages of the inverters for various values of Wp and Wn.

$$Vth = \frac{Vtn + \sqrt{\frac{1}{Kr}}(VDD + Vtp)}{1 + \frac{1}{\sqrt{Kr}}} \quad (1)$$

Where,
process trnsconductance of nMOS is given by,

$$Kn = un\ Cox \left(\frac{W}{L}\right)_n$$

and of pMOS it is

$$Kp = up\ Cox \left(\frac{W}{L}\right)_p$$

Tran conductance ratio Kr of the inverter circuit is given by,

$$Kr = \frac{K_n}{K_p} = \frac{u_n Cox \left(\frac{W}{L}\right)_n}{u_p Cox \left(\frac{W}{L}\right)_p}$$

LTE Comparator: LTE-Linear Transconductance Element comparator structure resembles TIQ comparator with extra two transistors as shown in Fig. 3. The sleep transistors are operated in linear region to achieve linear

transconductance operation. This relaxes the power bounds on inverter circuit reducing power consumption and hence improved Power Supply Rejection Ratio (PSRR). The operating range over input signal swing of this comparator is less. The operating range offered by this design is 0.866V to 0.885V of the input signal swing of 1.8V. The LTE comparator designed by varying Wn and Wp from 400nm to 2.5um in 180nm technology with supply voltage Vdd equal to 1.8V, consumes an average power of 0.740uW with Vg1 = 1.6V and Vg2 = 0.2V.

Figure 3: Linear Tunable Transconductance element comparator

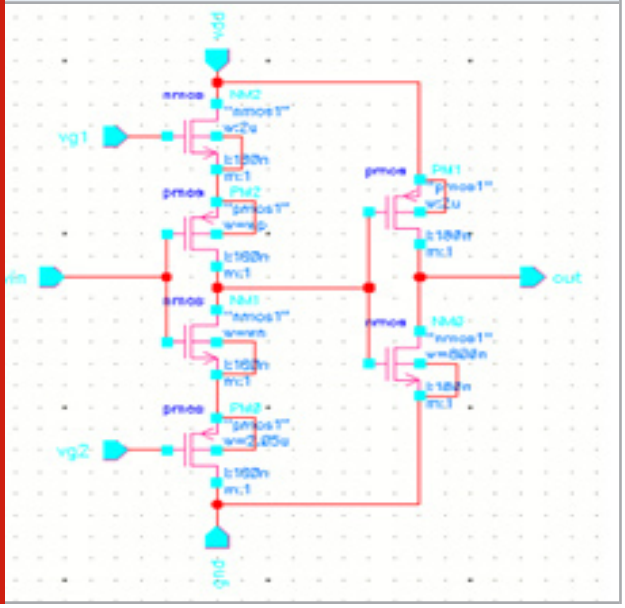
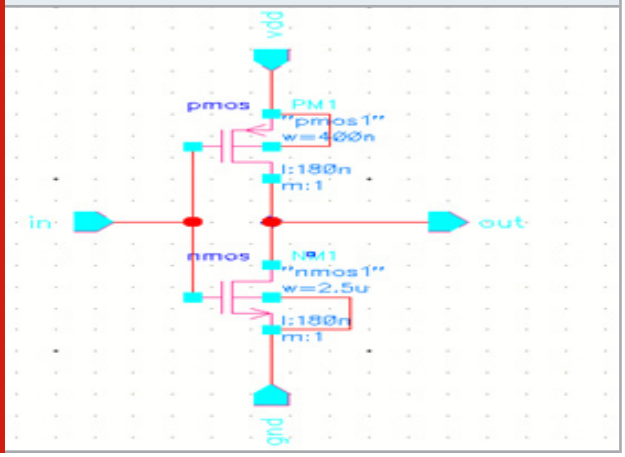


Figure 4: Single inverter comparator



Single Inverter Comparator: The inverter circuit can be used for generating different reference voltages by varying its 'Wp' and 'Wn' and comparing. The single inverter circuit generates the inverted outputs. The output is high when applied voltage is lesser than reference voltage generated by the inverter and becomes low when input is higher than reference voltage as in Fig. 4 shown below. This single inverter comparator operates from 0.615V to 0.932V of the input signal swing.

Single Inverter Comparator wit Reference Voltage: The above single inverter comparator operates almost over the entire input signal swing due to the reference voltage applied on the source terminal and reduces power dissipation by lifting the source voltage above ground. The threshold voltage values vary from 0.618V to 1.315V for Vref voltage values ranging from 0V to 0.771. The power consumption of this comparator varies with reference voltage; it is least for high reference voltages. The design with Vref = 0.771V given in Fig. 5 consumes an average power of 2.94pW.

Figure 5: Single inverter comparator with reference voltage

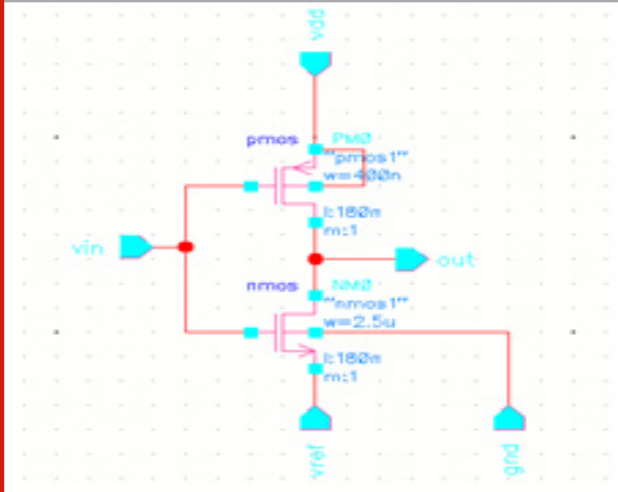
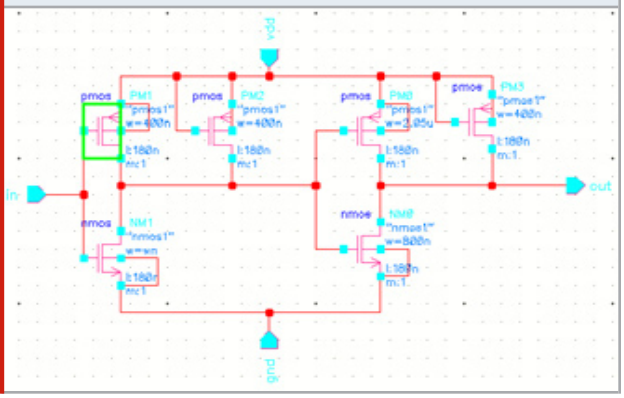


Figure 6: ITIQ comparator with reference voltage



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reference voltage; it is least for high reference voltages. The design with Vref = 0.771V consumes an average power of 2.94pW.

Improved TIQ Comparator: The improved TIQ comparator as in Fig. 6 has two extra p-transistors to get stable output of the comparator. These transistors will improve its performance and makes it more reliable. Table 1 gives the comparison between the various inverter based comparators. The simulation results show that single inverter and TIQ comparators are faster however with more power consumption. The LTE technique has better results but covers very little range of input signal swing.

Table 1. Comparison of Inverter based comparator circuits designed with 180nm Technology

Comparator	Input signal swing(Vin)	Avg. Power Dissipation	Delay
Single inverter	0.615V to 0.932V	5.647uW	28.22usec
LTE	0.866V to 0.885V	0.740uW	1.38usec
Single Inverter with (Vref = 0.771V)	0.618V to 1.315V	0.015uW	53.70usec
TIQ	0.59V to 0.930V	6.046uW	28.03usec
ITIQ	0.59V to 0.930V	6.042uW	28.02usec

Design of Encoder: Encoder is the digital part of Flash ADC which converts thermometer coded input to its equivalent digital output. For 3-bit Flash ADC the outputs of the corresponding thermometer codes are as indicated in the truth table as given in Table 2. The encoder is designed with following equations.

Table 2. Thermometer to Binary Code

Thermometer code	y2	y1	y0
1111111	0	0	0
1111110	0	0	1
1111100	0	1	0
1111000	0	1	1
1110000	1	0	0
1100000	1	0	1
1000000	1	1	0
0000000	1	1	1

In (Budanov, D. O.et al., 2018) proposed "high speed encoders" A high speed ROM encoder is designed in cadence tool with 180nm technology. Fig. 7 depicts the schematic diagram of ROM encoder. ROM encoders are faster and their delay is independent of the resolution. Where as in case of Wallace tree, Fat tree, and multiplexer based encoders the delay depends number of input bits. To achieve faster conversion irrespective of number of inputs ROM encoder is preferred. The circuit converts thermometer code to digital code with very high speed. The high speed ROM encoder is designed with following equations 2 to 4. Where y2, y1 and y0 are the outputs of the encoder and c1 to c7 are comparator outputs.

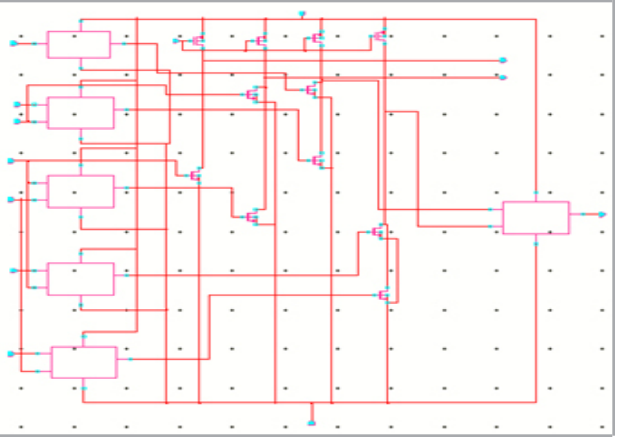
$$y2 = \overline{c4} \qquad \text{-----2}$$

$$y2 = \overline{c2 + \overline{c4}c6} \qquad \text{------3}$$

$$y0 = \overline{c7} + \overline{c1}c2 + \overline{c3}c4 + \overline{c5}c6 \qquad \text{----4}$$

We use two ROM encoders in this design as with TIQ we use normal encoder but in single inverter based we get complemented outputs hence ROM encoder designed for complemented comparator output is used with single inverter based circuits.

Figure 7: Schematic diagram of ROM Encoder.



RESULTS

The inverter based comparators are designed and simulated cadence design tool with 180nm technological library. The values of 'W' and 'L' are chosen by observing

the results of parametric analysis. The simulated outputs of circuits are depicted from Fig. 7 to Fig. 12.

Figure 9: Transient response of ITIQ based comparator block

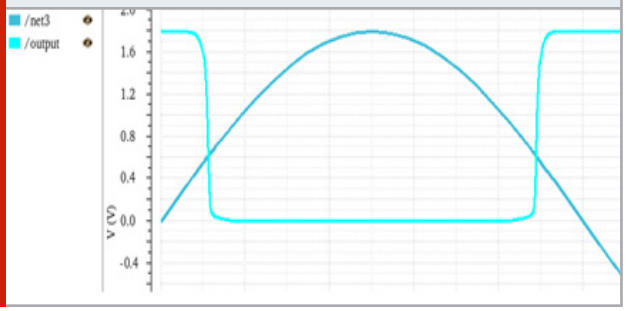


Figure 10: Transient response of Single inverter based comparator block.

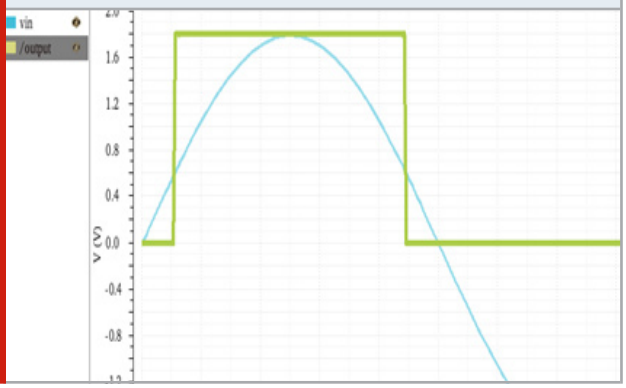


Table 3. Simulation results of Flash ADC designed with 180nm Technology.

Flash ADC	Avg. Power Dissipation	Delay
Single inverter comparator FADC	554.06uW	73.12usec
Single Inverter with ref. Voltage comparator FADC	459.8uW	2.832nsec
TIQ FADC	298.9uW	73.16usec

The simulation results in Table 3 shows that the power dissipation is less in TIQ comparator based Flash ADC circuits than single inverter circuits. The results also show single inverter with reference voltage Flash ADC is faster among inverter based Flash ADC circuits.

CONCLUSION

The inverter based comparator circuits are designed using cadence analog design tool for 180nm technology. The simulation results show that as reference voltage is applied at the source of nmos transistor, power consumption is significantly reduced however leading to more latency. As reference voltages applied are different, the delay and power consumption, vary with reference voltages. 3-bit Flash ADC circuits are designed with different inverter based circuits. The results show that power consumption is considerably reduced by using TIQ comparators. The results also show that whenever speed is the criteria than single inverter based Flash ADC is the better choice.

Figure 11: Transient response of TIQ based comparator block

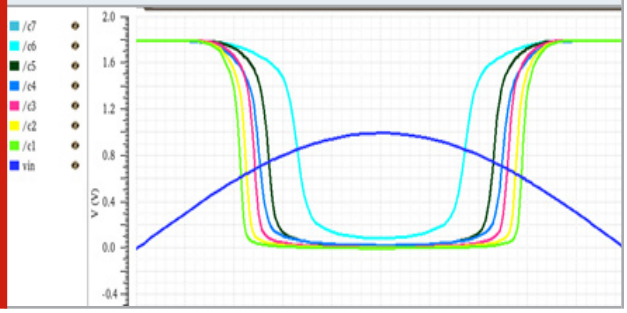


Figure 12: Transient response of designed 8:3 ROM Encoder

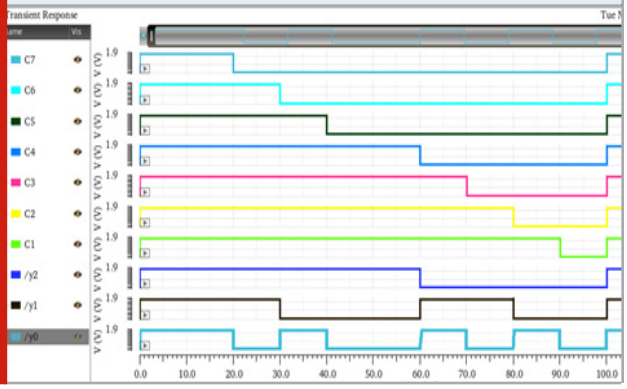
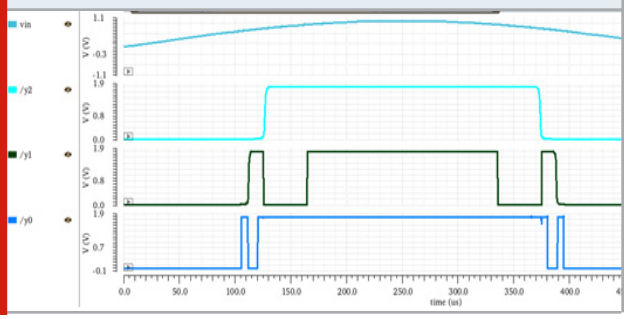


Figure 13: Output waveforms of 3-bit TIQ based flash ADC at 10MHz.



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