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Disigning A Novel Architecture to Reduce Stand by and Dynamic Power Dissipation for Sleepy Keeper Cmos Logic Circuits

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ABSTRACT

Scaling down of transistors will directly affects the decreasing in threshold voltage. Impact of decreasing threshold voltage is increasing in leakage current. In this paper many power gating circuits are discussed for their advantages and disadvantages, based on this literature survey a novel low power state retention technique is proposed in this paper. The proposed technique with its novel architecture reduces the leakage power (static power) and dynamic power dissipations. It also gives the state retained output. Performance of the proposed circuit is evaluated on some basic circuits in terms of their total and dynamic power dissipations. Extensive SPICE simulations were carried out and the results are compared with some existing techniques. Simulated results shows that proposed technique gives the efficient power minimization and state retained standby mode output.

KEY WORDS: FEEDBACK, HPG, LOW POWER, MTMOS, ON CURRENT.

INTRODUCTION

As the moor's law says that for every eighteen months the numbers of transistors on a silicon die are going to be double, now a day's the millions of transistors are accumulated on System on Chips (SoC).as the number of transistors doubles it also decreases the size of transistor and intern the power dissipation increases. It's not a severe problem in small circuits but as the circuit size and complexity increases, the high power dissipation diminish the battery life and also it requires the extra cooling and packaging costs.

$$P_{total}=P_{dynamic}+P_{shortcircuit}+P_{static} \quad (1)$$

From the above equation shows the sources of power dissipation.(1) Pdynamic due to switching activity of the input.(2) Pshortcircuit due to momentary conduction path between supply and ground .(3) Pstatic due to leakage current. The major design metrics in the VLSI circuit design are power and delay. As the supply voltage scales down the threshold voltage also should scale down. It increase the leakage current in exponential way. This increases the static power dissipation. One more design consideration is Output current that varies directly with the leakage current. As we decrease the output current, it intern decrease the leakage current but coming to the delay, propagation delay is inversely proportional to the output current as the output current decreases it increases the propagation delay.

So always there is a tradeoff between the delay and leakage power. There are many concepts for reducing

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the leakage power dissipation. Those are sleep transistor, body biasing methods and leakage control transistor methods and so on. These techniques were discussed for their merits and de merits in Material and Methods section. This Section also reveals the proposed design. In Result and discussion section shows the comparative results on Power dissipations of few combinational circuits. Last Section concludes this paper.

MATERIAL AND METHODS

In (Mutoh et al., 1995) proposed the MTCMOS technique, here high threshold header and footer sleep signal operated PMOS and NMOS are inserted for basic conventional circuit. And the low threshold transistors are chosen for base logic circuit. This technique is not suitable for low power circuits. This technique takes more delay and area to produce specified output. In (Drake et al., 2003) presented the Dynamic threshold CMOS technique, in this circuit base and gate of a MOSFETS are shorted, therefore dynamically it varies the threshold voltage by the concept of forward and reverse body biasing. The main drawback of this circuit is according to (Keshavarzi et al., 1999) reverse body bias leads to the steep rise in junction leakage current due to the technology scaling. In (Hanchate et al., 2004) author proposed the Lector technique.

This circuit is a self controlled one, but the drawback of this technique is output levels are not good. In (Kim et al., 2006) author put forward the sleepy keeper approach. This approach retains the state of output in standby mode. But main drawback of this circuit is increased area and wiring lengths leads to the more delay in output. In (Lakshmikanthan et al., 2006) authors recommended the new technique sleep circuit embedded CMOS circuit. This circuit avoids the draining of battery in the standby mode by producing the zero output, but the disadvantage of this technique is the concept of state retention is not maintained. In (Katrue et al., 2008) the GALEOR technique was proposed, this technique is a self controlled design with good leakage minimization but the main drawback is output signal levels are not good. Drain gating concept was presented in (Chun et al., 2010).

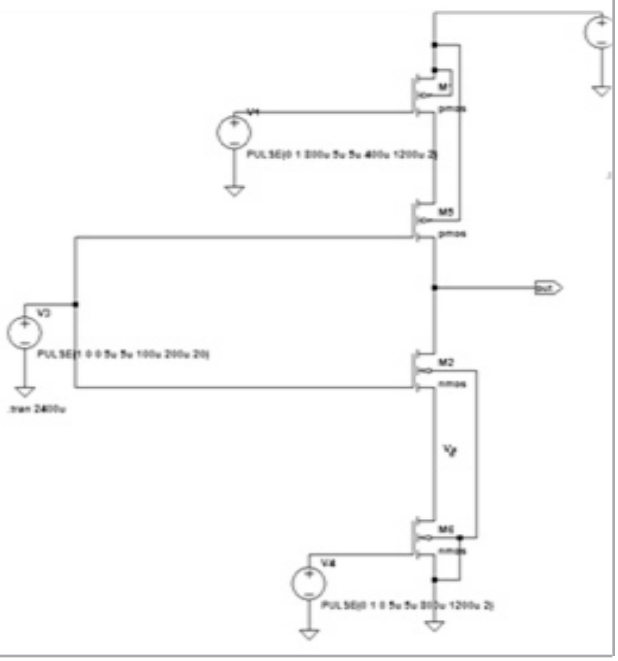
In this circuit power is gated at the drain side instead of at the source side. With this concept it remarkably reduces the dynamic power dissipation but not the static power dissipation. In (Chowdhury et al., 2012) authors projected a new variable body biasing technique. In this circuit the sleep transistor threshold voltage is increased from body biasing technique so, in turn it decreases the sub threshold leakage current. But main drawback is complexity and area gets increased from this extra body biasing circuit. A GLBB technique was recommended in (Corsonello et al., 2014). This circuit gives a good delay minimization, but at cost of increased area. In (Sharma et al., 2015) it was proposed the new technique called ONOFIC. In this circuit delay and power will be get reduced from a feedback PMOS transistor.

Appropriate selection of input signal can give a better leakage minimization, but selection of input signal is needed to be done by algorithms which take extensive computational time. New LCNT approach was found by (Lorenzo et al., 2017). this circuit reduces the leakage power with a series connected two NMOS transistors in between output and pull down circuit. With the cost of less quality signal levels. In (Johannah et al., 2017) authors recommended the hybrid power gating technique, as discussed in further section it decreases the leakage power dissipation through sleep transistor stacking effect and through PMOS feedback transistor and reverse body bias technique is used to further reduce the leakage power dissipation. This feedback PMOS transistor feeds back the leakage current to input. This will reduce the dynamic power dissipation.

Proposing A New Low Power Technique: To achieve Low power dissipation in CMOS circuits, they will be incorporated by few leakage control transistors.

MTCMOS: Let us take a conventional inverter circuit. For this circuit M1 PMOS is connected between power supply and pull up circuit. This circuit controlled from V2 (sleep signal) voltage source. The M4 NMOS is connected between pull down and ground. The M4 NMOS is controlled from V3 (complement of sleep signal) voltage.

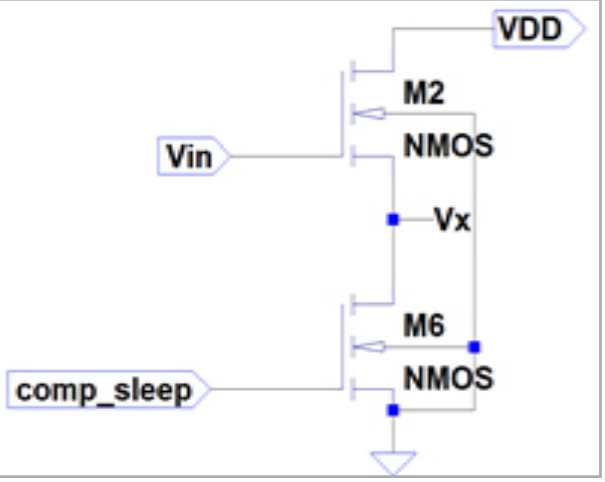
Figure 1: MTCMOS circuit



The Multi Threshold CMOS circuit will reduce the static power dissipation by reducing leakage power in sub threshold region. Because Pull down is not directly connected to the ground but through the virtual ground. It has the node potential Vx greater than ground potential.

Calculation of Vx

Figure 2: Analysing stack effect



In sleep mode sleep signal is high. Comp_sleep is '0' and when Vin='0'. From Low power methodology manual: for system-on-chip design and Scaling of stack effect and its application for leakage reduction proposed by (Flynn et al., 2007; Narendra et al., 2001) Modified the standard leakage power equation by replacing ex component by 10x component.

$$I_{leakage}=I_{off}10^{\frac{Vgs-Vtho-K_\gamma Vsb+\eta Vds}{S}} \quad (2)$$

Where I off is the sub threshold leakage current at V_{gs}=0, assume V_{tho}=0 threshold voltage at zero bias condition and V_{ds}=Vdd, S is sub threshold slope, η is DIBL coefficient K_γ is body effect coefficient. From stack effect analyzing circuit (Fig.2). Leakage current of M2 and M6 transistors are given by

$$I_{leakM1}=I_{off}\ 10^{\frac{-Vx-K_\gamma Vx+\eta(Vdd-Vx)}{S}} \quad (3)$$

$$I_{leakM6}=I_{off}\ \ 10^{\frac{\eta Vx}{S}} \quad (4)$$

Vx is obtained by equating I_{leak}M1 and I_{leak}M6 because M1 and M6 are two series connected MOSFETS, so same current is flows in both the transistors.
Therefore,

$$-Vx - K_\gamma Vx + \eta(Vdd - Vx) = \eta Vx$$

Vx can be obtained as,

$$Vx = \frac{\eta Vdd}{1+2\eta+K_\gamma} \quad \ldots\ldots\ldots\ldots\ldots (5)$$

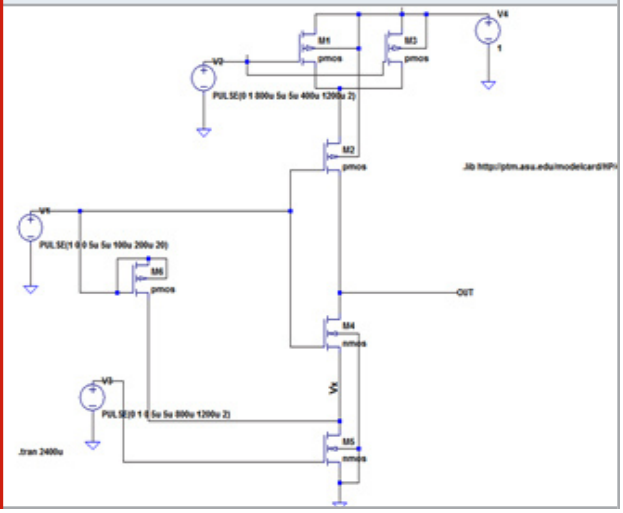
Substituting equation (5) in (3) or (4)

$$I_{stack} \simeq I_{off}\, 10^{\frac{\eta Vdd}{S}} \quad \ldots\ldots\ldots\ldots\ldots (6)$$

According to (Kavitha et al., 2016) assume s=100mv/decade and η=100mv/v for 65nm technology. By substituting these values in Istack. It shows stacking effect will minimize the leakage current by a factor of nearly 10.It shows decrease in leakage current will reduce the leakage power dissipation in turn static power dissipation.

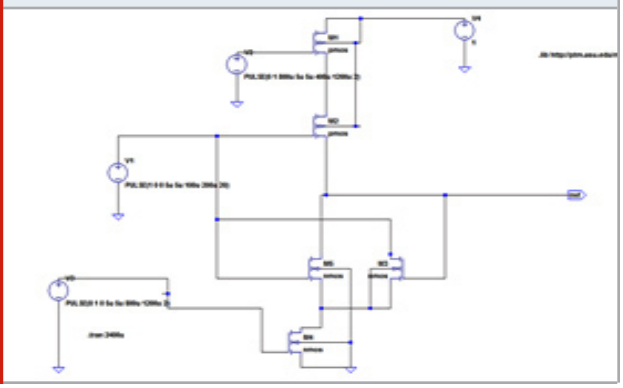
Novel Hybrid Strucure: In (Johannah et al., 2017) authors recommended architecture i.e. novel hybrid structure.

Figure 4: Novel hybrid inverter



On the basic MTCMOS circuit, this Novel Hybrid structure is evolved. The extra PMOS M6 is added in the path from Vx to V1 (input voltage).V1 acts as drain and gate of M6.In active mode, when V1 (input) ='0' all PMOS transistors M1, M2, M3 and M6 are conducting and NMOS M4 is in OFF state. This combinations of inputs gives Vout=VDD. When N1 is in OFF state it tries to pull down the Vout through OFF state leakage current. Even this current is small due to stack effect which discussed previously; this little leakage current will flow from Vx to V1. This reduces the ON current of PMOS M3 and thereby reducing the dynamic power dissipation to maintain this PMOS M3 in ON state, in this way the novel Hybrid structure reduces the leakage and dynamic power dissipation.

Figure 4a: Proposed technique



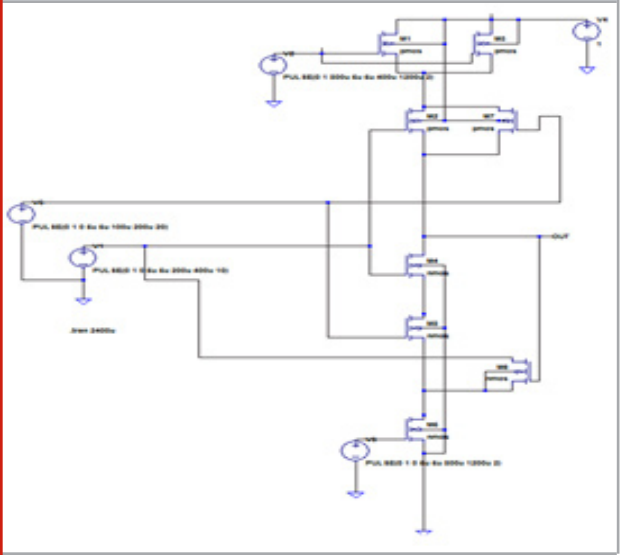
Proposed Technique: The proposed technique combines the MTCMOS and Novel Hybrid structure to reduce the

leakage as well the dynamic power dissipation as shown below.

The proposed technique is also evolved from the MTCMOS architecture. Advantages of MTCMOS architecture are
1) It incorporates the sleep transistors for standby mode of operation.
2) This architecture retains its state when it comes out from standby mode.
3) From these sleep transistors leakage power dissipation reduces effectively.

In Novel Hybrid structure the dynamic power dissipation is reduced through feedback PMOS transistor. This feedback PMOS is connected between virtual ground and ground node to input voltage, to feed back the leakage current to input. In similar way the proposed technique [Fig.3] feedback path from Vx to V1(input) is constructed from NMOS M3 .whenever the input is '0' the output becomes 'Vdd' this Vout is gate voltage for the for the proposed design feedback NMOS M3 transistor. Due to Vout=Vdd the NMOS M3 gets ON. Whatever the leakage current flowing in Vx node is fed back to input through this NMOS M3 transistor, like this way it increases the ON current of Pull Up PMOS M2.both Proposed and Novel Hybrid inverter structure are used to decrease the static power dissipation through stack effect, to retain the output state after sleep mode using header and footer sleep transistors and to reduce the dynamic power dissipation through feedback transistors.

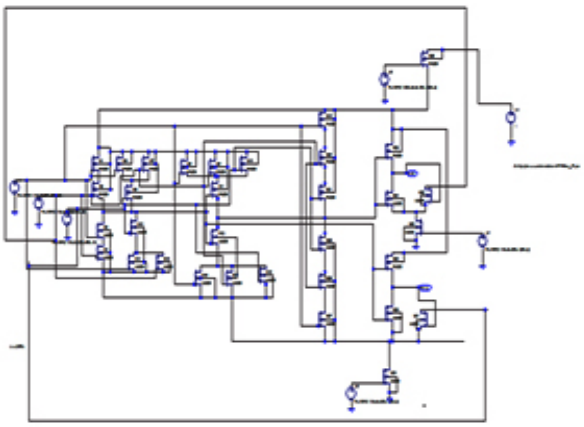
Figure 5: Proposed NAND gate



Advantages of proposed technique over Novel Hybrid structure.
1. The proposed design will efficiently reduce the total power dissipation by reducing the dynamic power dissipation. This is analyzed by PMOS versus NMOS as feedback transistors. In (Shuler 2017) it was strongly recommended that PMOS transistors, due to the use of holes rather than electrons as carriers are slower and carry less current. As a result of the latter they must be two to three times larger to balance with paired NMOS transistors. For radiation events, the PMOS transistors are simply larger and slower and contain more charges and are therefore harder to upset. So, the larger PMOS transistor is inefficient compared to NMOS transistor.

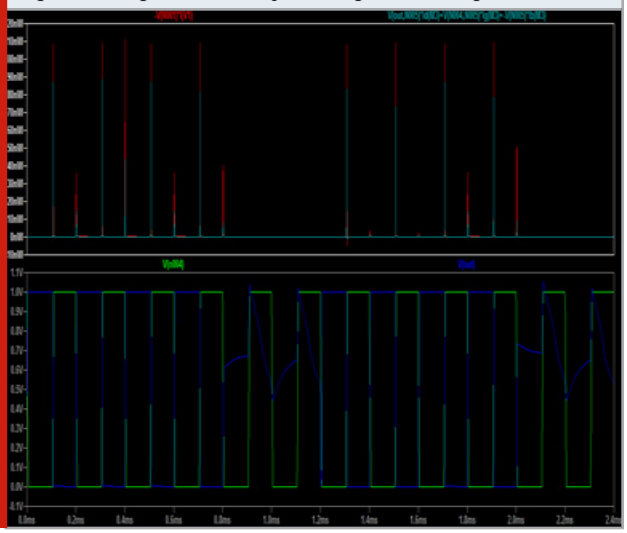
2. Another disadvantage of Novel Hybrid structure is using of reverse body biasing in feedback PMOS to reduce further leakage power. It's known that using the reverse body bias will increase the stress on the device. Over the time it decreases the performance as well the life time of a device. One of drawback it is observed from the reverse body biasing is decreasing of break down voltage of a device. But proposed architecture is free from reverse body biasing effects.

Figure 6: Proposed One bit full adder



In the proposed NAND gate the virtual ground is connected to the source of the feedback transistor and drain is connected to any one of the input.

Waveform 1. Proposed inverter logic circuit output with input, total power and dynamic power dissipations.



In the proposed one bit full adder circuit leakage current at the SUM output is fed back to the V2 input and leakage current at the carry output is fed back to the one more

input V3.using this leakage current feed backing concept it noticeably reduces the total power dissipation.In the proposed one bit full adder circuit leakage current at the SUM output is fed back to the V2 input and leakage current at the carry output is fed back to the one more input V3.using this leakage current feed backing concept it noticeably reduces the total power dissipation.

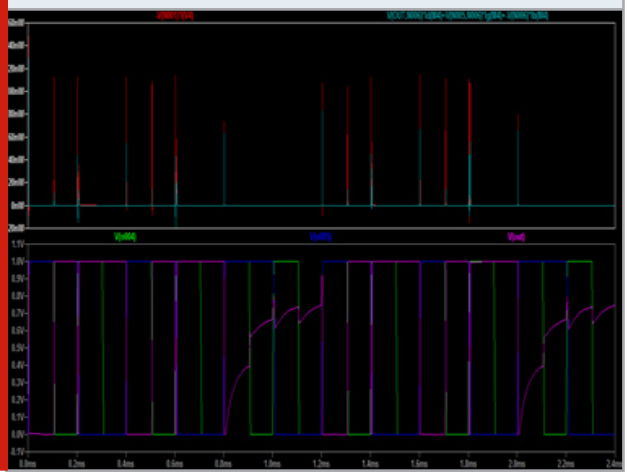
Table 1. Comparison of power dissipation in Inverter circuit using different architectures

sl.no	Design architecture	Average total power dissipation (over 2.4ms)	Average dynamic power dissipation
1	Conventional	608.8pW	333.8pW
2	MTCMOS	397.44pW	185.98pW
3	Sleep circuit Embedded CMOS circuit	496.6pW	247.68pW
4	Drain gating	439.6pW	86.3pW
6	Variable Body bias Technique	376.65pW	185.98pW
7	Novel Hybrid Gating	373pW	197.96pW
8	Proposed Design	362pW	75.74pW

Table 2. Effect of technology scaling on total and dynamic power dissipation in proposed technique

sl.no	Different Technology nodes	Scaled downed Supply voltage	Average Total power dissipation (over 2.4ms)	Average Dynamic power dissipation
1	45nm	1.1V	853.79pW	198.27pW
2	32nm	1V	297.52pW	57.29pW
3	22nm	0.9V	52.3pW	11.47pW
4	16nm	0.8	26.5pW	6.2pW

Waveform 2. Proposed NAND logic circuit output with input, total power and dynamic power dissipations.



RESULTS AND DISCUSSION

The inverter logic circuit is implemented using 45nm technology (taking from Low Power PTM library files) and by applying the 1V power supply in LTspiceXVII.

From the Table 1, it proves that the total as well dynamic power dissipation will be considerably reduced as compared to other architectures.

From the above comparison Table 2, it is observed that, with technology scaling proposed low power architecture works well to reduce the total as well dynamic power dissipation remarkably.

Waveform 3. Resultant waveform of the proposed One bit Full Adder

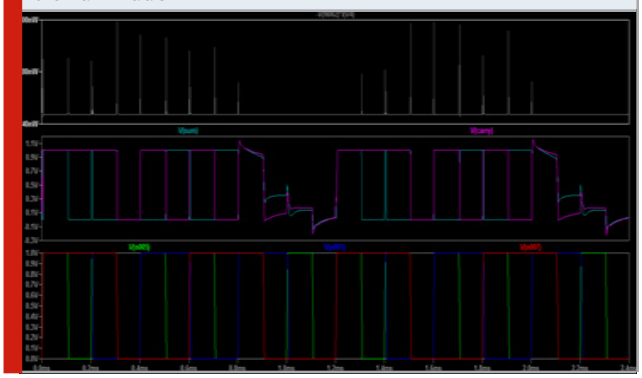


Table 3. Comparison of average total power and dynamic Power dissipation in NAND logic circuit constructed from Different design architectures.

sl.no	Design Architecture	Average Total power dissipation (over 2.4ms)	Average Dynamic power dissipation
1	Conventional	648.46pW	291.25pW
2	MTCMOS	438.22pW	173.99pW
3	Novel Hybrid Gating	433.01pW	139.62pW
4	Proposed NAND gate	288.74pW	29.9pW

Table 4. Comparison of average total power dissipation in Designing One bit full adder using low power 45nm technology.

sl.no	Design Architecture	Average Total power dissipation (over 2.4ms)
1	Conventional one bit full adder	2.371nW
2	Proposed one bit full adder	812.53pW

CONCLUSION

The aim of VLSI circuit design is to miniature the electronic circuits and in turn to reduce the power dissipation. As the technology scales down it decreases the threshold voltage which leads to the increase in leakage power. In this paper, through literature survey many leakage power techniques are analyzed to find there advantages and disadvantages. These techniques are compared with proposed power reduction technique. We found the proposed technique gives relatively good dynamic and total power reduction. In future we can implement this technique to design a low power processor.

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