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Simulation and Analysis of Reduced Switch Multilevel Inverters for High Power Applications

Rakesh B Halligudi[1], Uma Kulkarni[2] and Shivanand Killedar[3]
[1,2,3]Department of Electrical and Electronics, KLE DR M S Sheshgiri
College of Engineering and Technology, Belagavi, India

ABSTRACT

This paper presents the Envelop Type (E-Type) reduced switch modified multilevel inverter. Each module of this inverter produces thirteen levels of output voltage using four voltage sources and ten switches. The main advantage of this topology is its ability to produce the negative voltage levels without the H-bridge inverter. The topology is compared with other recently developed reduced switch modified multilevel inverter (MLI) with number of switches and number of DC sources required and there is a substantial reduction in the total number of devices. This in turn reduces the area and the power dissipation. Reduced power dissipation means reduced the heat loss and efficient heat sinking is possible. This topology is designed in MATLAB and simulated using Simulink. Selective Harmonic Elimination (SHE) methodology is applied to get less distorted and stable output voltage. Total Harmonic Distortion (THD) is reduced to 3.46 % as compared to 7.7% attainted using reduced carrier PWM methodology. The same topology with RL load showed a THD of just 0.84% for the current waveform reproducing exact sinusoidal waveform. This can be appreciated in large load systems. Another observation made shows that the voltage stress across each of the switches is reduced which in turn reduces the switching losses. This allows the user to use low rating devices comparatively.

KEY WORDS: MODULAR MULTILEVEL INVERTERS, MULTI LEVEL INVERTERS (MLI), REDUCED SWITCH CONVERTERS, SELECTIVE HARMONIC ELIMINATION, TOTAL HARMONIC DISTORTION (THD).

INTRODUCTION

The ever growing demand for electrical energy has led to the exploration of available renewable energy resources. Solar and wind energy are the most commonly used renewable energy resources in India. They are extremely unpredictable, despite the fact that they are plentiful in nature. Instead of their high dependence on different environmental factors, solar and wind power in particular are two most popular renewable sources. Their adaptation to the existing system is a huge task, hence creating research interest among power electronics and the power system community (Ellaban et al., 2014; Akram et al., 2017; Kumar et al, 2017). The inverter which forms main part of renewable energy sources transforms the solar DC power into custom AC power. In domestic and small-scale industries, traditional two/three-level inverters are used (Mathew et al., 2012). However these conventional inverters produce highly distorted output voltage, thus requiring bulky grid integration filters.

The switching losses are high since these inverters use high frequency PWM switching technique in order to eliminate the lower order harmonics. The existing renewable energy system make use of the conventional MLI (Diode clamped MLI, Flying capacitor MLI, Cascaded H-Bridge MLI). Cascaded H-Bridge MLI (CHB MLI) is popular for solar applications because of its modular design and low voltage stress across the switches. The main benefit of CHB MLI is that they produce less distorted output
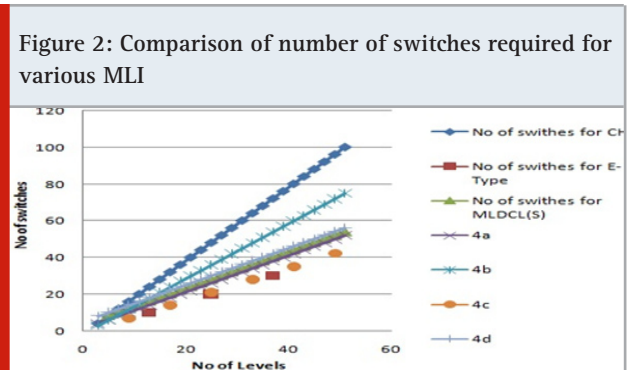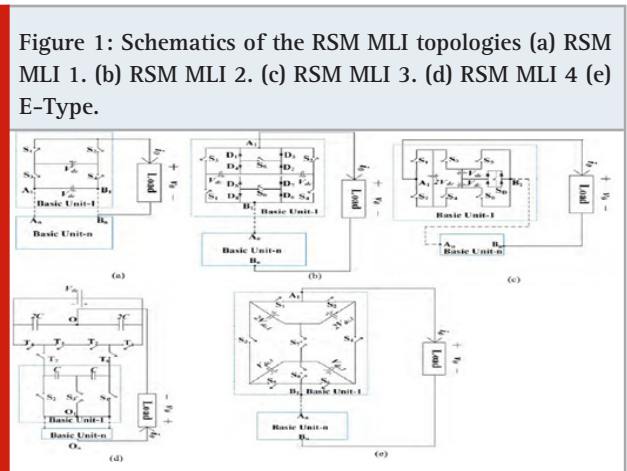
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voltage. It can be operated at the required frequency starting from fundamental frequency. The key downside of CHB MLI is that the number of switches drastically increases with increase in the number of levels that is 2 (n-1) switches are required for a N level inverter.

Reduced switch converters are proposed to address the drawbacks of CHB MLI. Researchers are now focusing on reducing the number of devices. The reduction in the total number of switches, diodes, capacitors, and voltages sources has increased the reliability of inverters .This also minimizes overall cost and losses leading to a stable and economical design (Bana et al.,2019). Several new reduced switches MLI topologies have been recently developed with several improvements and the research is still on.

A. E–Type Reduced Switch Converter: The reduced switch converters are available in more than one configuration and are classified as
1. Reduced switch symmetric type MLI (RSS MLI)
2. Reduced switch asymmetric type MLI (RSA MLI)
3. Reduced switch modified MLI (RSMMLI)

Several types are also developed in the above three configurations and are being tested for required metrics. RSMLI topologies are shown in (Figure 1).The number of switches required for the various MLI configurations is compared and the graph of the same is shown in (Figure 2). It can be observed that the number of switches required for the envelope type is very less compared to the other topologies indicated in the (Figure 2).

Figure 1: Schematics of the RSM MLI topologies (a) RSM MLI 1. (b) RSM MLI 2. (c) RSM MLI 3. (d) RSM MLI 4 (e) E-Type.

Figure 2: Comparison of number of switches required for various MLI

B. Configuration of Envelope Type MLI: The Envelope Type (E-Type) reduced multilevel inverter has been first proposed in a paper published in 2016(Samadaei et al., 2016). Each module of E-Type produces 13 levels of output voltage ie (0 to ±6Vdc) with 10 switches and 4 uneven DC voltage sources with two of them being Vdc and the other two twice Vdc. The main advantage of this module is its ability to generate negative voltage level without the H-Bridge circuit which is not the case with other RS MLI. Thirteen voltage levels are obtained by connecting the voltage sources (Vdc, twice Vdc) in series by means of the switches.

Fig 3arepresents a single module of E-Type Reduced Switch MLI and figure 3b shows cascaded configuration. The switch S7 which is bidirectional is essential to avoid the short circuit of the DC sources on either side of the module. The Switch S8 is required to generate ±5V voltage level. (Table 1) shows the switch status for the different voltage levels. The paths to obtain different voltage levels are selected in such a manner that positive of the DC Voltage are never connected to positive of the diode. Thus short circuiting of the DC sources can be avoided.

Table 1. Switching Table

X*(Vdc)	S1	S2	S3	S4	S5	S6	S7	S8
1	1	0	0	0	0	1	1	0
2	1	0	0	0	0	0	1	1
3	1	0	0	0	1	0	1	0
4	1	0	0	1	0	1	0	0
5	1	0	0	1	0	0	0	1
6	1	0	0	1	1	0	0	0
0	1	0	1	0	1	0	0	0
−1	0	1	0	0	1	0	1	0
−2	0	1	0	0	0	0	1	1
−3	0	1	0	0	1	1	1	0
−4	0	1	1	0	1	0	0	0
−5	0	1	1	0	0	0	0	1
−6	0	1	1	0	0	1	0	0
Number of turning on /cycle	1	1	3	1	7	7	4	8

C. Extension of E Type MLI: The required number modules can be connected in series to produce additional number of voltage levels which is given by the 12n+1. Two E-Modules are connected in series is shown (Figure 3b) which can generate 25 voltage levels.(0 to ±12Vdc). Table 2 presents the voltages of each module in terms of Vdc to obtain 25 different levels of output voltage. Each voltage level will have several paths like voltage level 1, 1Vdc has twelve different paths while 2Vdc will have only eleven paths and so on so forth is also indicated in Table 2) (Bana et al.,2019).The alternative paths for the same voltage levels increases the eliability of the MLI. This is because these alternate paths can be chosen in

case of failure of a switch or its river circuit and also to equalize the stress.

Figure 3 a: Single module of E-TYPE MLI b. Cascade module to produce 25 Levels
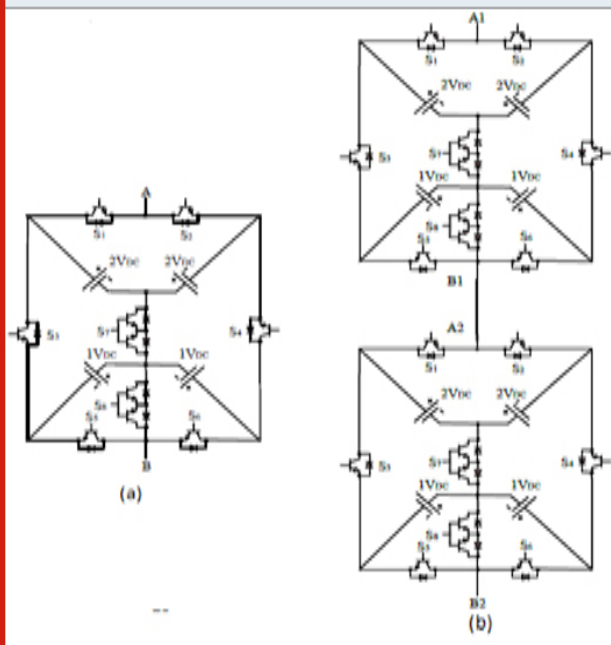
D. Voltage Control Schemes: There are two types of voltage control schemes available for the RSMLI. One of these is the high frequency Pulse Width Modulation (PWM) and the other is fundamental/low frequency switching. In PWM switching the following schemes are available like Level Shifted PWM (LSPWM), Phase Shifted PWM (PSPWM) and Space Vector PWM (Lee, 2018). In PWM scheme the switches are operated at a very high frequency and the output voltage is by controlled controlling the amplitude of the pulse. These LSPWM and PSPWM techniques cannot be applied directly to E type MLI because of variation in conduction levels. Hence reduced carrier PWM scheme with unified logical expressions is proposed for E type .This technique is applied to E-Type giving a THD of 7.7% (Vemuganti et al., 2018).

The main drawback of this technique is the high switching losses and high frequency switching harmonics present in the output voltage. Fundamental or low-frequency switching can provide better performance as compared to high-frequency PWM switching techniques (Sandeep and Yaragatti , 2017). The key forms of Fundamental Switching Schemes are Selective Harmonic Elimination (SHE) and Nearest Level Control (NLC). Of which SHE PWM-based techniques will potentially provide the highest quality performance (Nalcaci and Ermis, 2018).

Table 2. Alternative paths to generate Voltage Levels of cascaded E–Type MLI

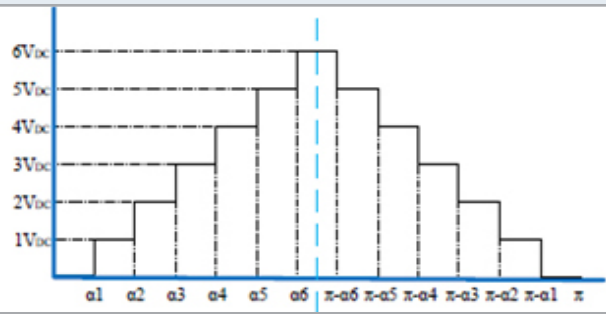| U1 → / U2 ↓	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6
-6	-12	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0
-5	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	1
-4	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2
-3	-9	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3
-2	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4
-1	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5
0	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6
1	-5	-4	-3	-2	-1	0	1	2	3	4	5	6	7
2	-4	-3	-2	-1	0	1	2	3	4	5	6	7	8
3	-3	-2	-1	0	1	2	3	4	5	6	7	8	9
4	-2	-1	0	1	2	3	4	5	6	7	8	9	10
5	-1	0	1	2	3	4	5	6	7	8	9	10	11
6	0	1	2	3	4	5	6	7	8	9	10	11	12

In case of SHE the step angle for the waveform have to be accurately calculated to reduce unique low-order harmonics. For this Fourier equations of the waveform must be solved which is a computational difficulty and if implemented requires complex hardware. To reduce this computational burden, optimization techniques like Colonial Competitive Algorithm (CCA), Genetic Algorithm (GA), Bee Algorithm (BA), Cuckoo Search Algorithm (CSA), Particle Swarm Optimization (PSO),

Bat Optimization Algorithm (BOA) have been used to solve SHE equations.(Memon et al., 2017).

E. Design snd Simulation of E–Type MLI: The inverter module is designed and simulated in MATLAB SIMULINK to validate the performance of E type MLI. This paper uses the Selective Harmonic Elimination Modulation (SHE-PWM) technique to construct a pulse pattern for the inverter. Different step angles α1 to α6 are

determined using the equations1 and its extensions (2 to 10). The angles obtained are shown in (Table 3). The output waveform obtained is shown in figure 4 is required to minimize THD and hence the simulations are validated.

Table 3. Stepping angles in degrees for modulation index ma=0.98

α1	α2	α3	α4	α5	α6
5.097	16.065	22.027	33.499	50.057	63.057

Figure 4: Generated output voltage to find αi to eliminate the desired harmonics

$$f_n(t) = \frac{a_n}{2} + \sum_{n=1}^{n} a_n \left(\cos\left(\frac{2\pi nT}{T}\right) + b_n \sin\left(\frac{2\pi nT}{T}\right) \right) \quad \text{......(1)}$$

$$b_n = \frac{4V}{n\pi} \sum_{i=1}^{i} (\cos(n\alpha_i)) \quad \text{......(2)}$$

$$b_1 = \frac{4V}{1\pi} [\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) + \cos(\alpha_5) + \cos(\alpha_6)] \quad \text{......(3)}$$

$$b_3 = \frac{4V}{3\pi} [\cos(3\alpha_1) + \cos(3\alpha_2) + \cos(3\alpha_3) + \cos(3\alpha_4) + \cos(3\alpha_5) + \cos(3\alpha_6)] = 0 \quad \text{......(4)}$$

$$b_5 = \frac{4V}{5\pi} [\cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) + \cos(5\alpha_5) + \cos(5\alpha_6)] = 0 \quad \text{......(5)}$$

$$b_7 = \frac{4V}{7\pi} [\cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \cos(7\alpha_4) + \cos(7\alpha_5) + \cos(7\alpha_6)] = 0 \quad \text{......(6)}$$

$$b_{11} = \frac{4V}{11\pi} [\cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) + \cos(11\alpha_4) + \cos(11\alpha_5) + \cos(11\alpha_6)] = 0 \quad \text{......(7)}$$

$$b_{13} = \frac{4V}{13\pi} [\cos(13\alpha_1) + \cos(13\alpha_2) + \cos(13\alpha_3) + \cos(13\alpha_4) + \cos(13\alpha_5) + \cos(13\alpha_6)] = 0 \quad \text{......(8)}$$

$$b_{17} = \frac{4V}{17\pi} [\cos(17\alpha_1) + \cos(17\alpha_2) + \cos(17\alpha_3) + \cos(17\alpha_4) + \cos(17\alpha_5) + \cos(17\alpha_6)] = 0 \quad \text{......(9)}$$

$$b_{19} = \frac{4V}{19\pi} [\cos(19\alpha_1) + \cos(19\alpha_2) + \cos(19\alpha_3) + \cos(19\alpha_4) + \cos(19\alpha_5) + \cos(19\alpha_6)] = 0 \quad \text{......(10)}$$

F. Comparison of the Obtained Results with Other MLI: The results of the E-Type topology are compared with CHB and topologies of RSM MLI and are shown in (Table 4). It is seen that E-Type MLI requires 10 switches for 13 levels of voltage but CHB MLI requires 24 switches which is more than double. E-Type MLI requires 4 DC sources to generate 13 levels of voltage. CHB MLI requires 12 DC sources. Hence we can conclude that E type is efficient in terms of area and also the THD level.

G. Matlab Model and Simulation Results: The Mat Lab Simulink model of E-Type MLI is shown in figure 5. The input pulses for the model are divided into two sets of four pulses (S1 to S4) and (S5 to S8) each for better visibility and are shown in the (Figure 6) and (Figure 7). The simulation was done using voltage step of 50 V each and frequency of 50Hz. The simulation is performed using R and RL type of loads. (Figure 8) is the simulation result of R type load with R=150 Ω. (Figure 9) is the output voltage waveform obtained for RL load with R=150 Ω and L=240mH. (Figures 9) and (Figure11) shows the FFT analysis for the both R and RL loads. THD for voltage of 3.46% and for current in the inductive load is 0.084%. Both of the values are (<8%) well within the standard limits mentioned for single phase system. The same MLI can be used in a three phase system where in the multiples of 3rd harmonic can be naturally eliminated and hence the total THD will be reduced further.

Table 4. Comparison E type with CHB and other RSM MLI.

Parameter	CHB	1a	1b	1c	1d	E Type MLI
Ndc	(N−1)/2	(N−1)/2	(N−1)/2	3(N−1)/8	1	(N−1)/3
TSV	2(N−1)	2(N−1)	5(N−1)/2	13(N−1)/16	(N+9)/4	5(N−1)/3

Figure 5: Simulink model of E-Type MLI for R load
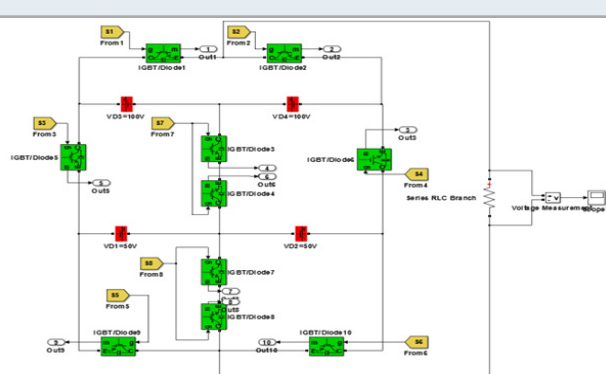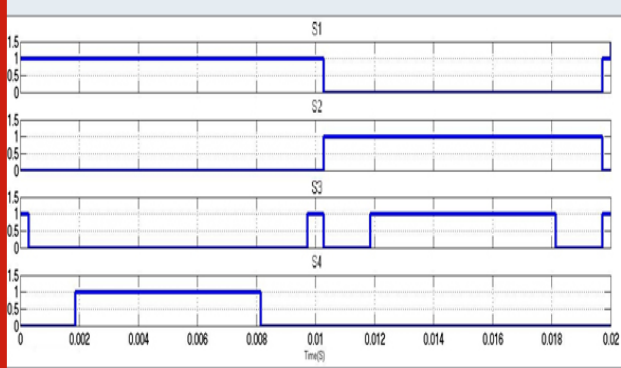

Figure 6: Switching pulses S1 to S4
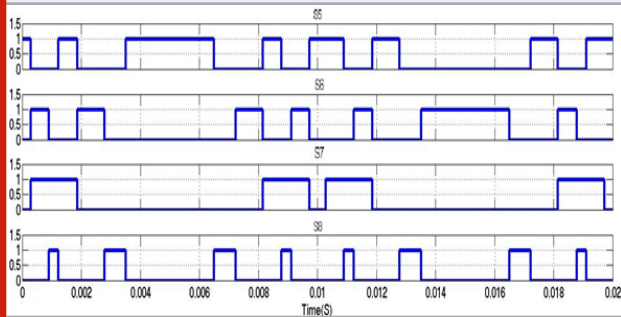

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Figure 7: Switching pulses S5 to S8

Figure 9: FFT analysis of output voltage

Figure 8: Output voltage for R=150Ω

Figure 10: Output voltage and output current for R=150Ω,L=240mH, PF=0.9
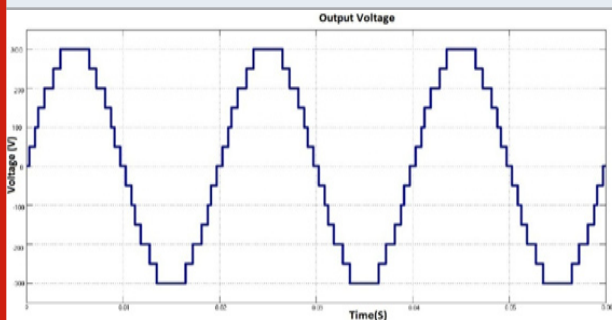

Figure 11: FFT analysis of output current with R-L Load.
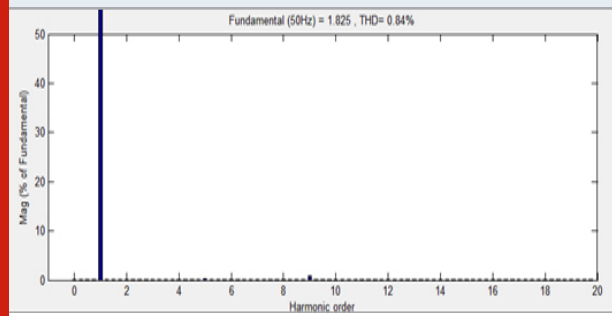

Table 5. Comparative Results

Voltage control Scheme	THD of phase voltage for R load.	THD of phase Current waveform for R-L load
Reduced carrier PWM scheme with unified logical expressions	7.7%	-
SHE-PWM	3.46%	0.84%

CONCLUSION

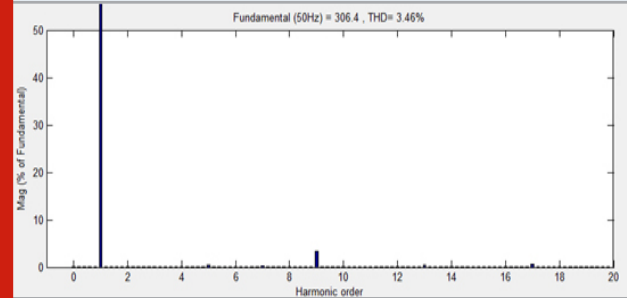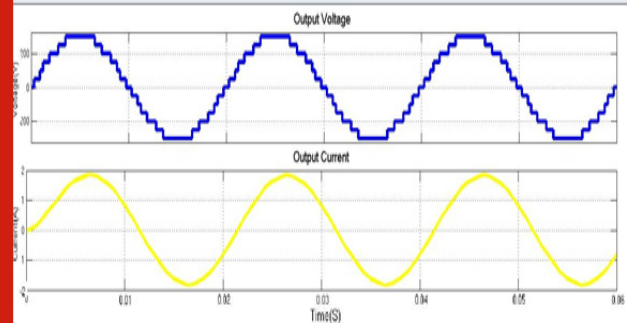E-Type RSMLI is successfully designed and simulated in MATLAB for R and R-L load. The topology is simulated using Selective Harmonic Elimination method, for the suppression of lower order harmonics. The THD of voltage for R load is 3.46% and THD of current for R-L load is 0.084 % and is well within the specified standards. The THD with RSC MLI topology is 2.8% for an AC load obtained from previous papers. This can be compared to RL results in this paper which is just 0.084% showing substantial improvement. Papers have been published with SHE-PWM topology and THD results reported is 3.46% which is again larger than the results obtained in this paper. Therefore it can be observed that the E type RSMLI as modeled here shows much better performance. The other advantage of this topology is its ability to generate negative voltages without H-Bridge. Compared to other RSM MLI this topology has low device count and low voltage stress. This makes topology best suited for high power application. It can be easily modularized to generate more number of voltage levels.

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