Biosc.Biotech.Res.Comm. Special Issue Vol 13 No 14 (2020) Pp-481-486

BBRC
Bioscience Biotechnology Research Communications

# Fault Tolerant Triple Modular System Using FPGA

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## ABSTRACT

Fault Tolerant Triple modular Redundancy is a Real-Time Reliable Concept that improves the performance of the systems by reducing the faults in the system. Triple Modular Redundancy is widely used in dependable systems to design high reliability against soft errors. This Experiment defines an approach towards a fault tolerant system using FPGA. Redundancy is an idea that is a copy of the currently implemented design. The proposed system is based on the concept of considering the majority of the real-time system and then giving the output of the system based on the ratio. This System allows us to detect which individual module in the system is at a fault. Triple Modular Redundancy develops a robust system towards Faults. This paper focuses on the implementation of triple modular redundancy on FPGA's and connecting the systems with the help of SPI communication. This paper illustrates how the TMR will be used to speed the fault analysis and use the system in Real-Time Applications and Environment. In this experiment, we use the FPGA system that ensures proper synchronization between the master and the slaves. The scope of his paper embraces the development of TMR various currently ongoing projects related to TMR, Recent projects developed with the help of TMR, Research going on in this field, disadvantages of the systems currently used in projects and appliances, and how Fault Tolerant Triple Modular System using FPGA will be able to solve the problem and can be implemented in the new systems and the test bench, software algorithms, functional simulations, timing simulations in Experiment.

**KEY WORDS:** FPGA, MISO, MOSI, REDUNDANCY, SPI, TMR.

## INTRODUCTION

The Fault Tolerant Triple Modular System Designed with the aim to reduce the faults in the system and achieve task correctness. Triple Modular Redundancy is one of the most commonly used fault tolerant techniques which is mostly used in FPGA. As the probability of faults reduces the reliability of the system increases. At present, the use of real-time system in critical applications like aviation, space exploration, nuclear plants, the manufacturing sector has increased tremendously. For real-time applications the fault tolerant system the minimum performance overhead is very important. For a system to be reliable the system should be equipped with appropriate error detection and meeting the timing constraints.

Error in the system is a sign of fault and a single error may result in numerous faults. Because of the above-mentioned functionality requirements, the FPGA has become a platform to be selected because of their high performance in signal processing tasks, short design process time in developing a system having high complexity [1]. The flexibility and performance make FPGA the choice. FPGA boards using Static RAM feature are reconfigurable and the programs in the device can be changed as the requirements change. FPGA and their

ARTICLE INFORMATION

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*Received 14th Oct 2020 Accepted after revision 29th Dec 2020*
*Print ISSN: 0974-6455 Online ISSN: 2321-4007 CODEN: BBRCBA*

*Thomson Reuters ISI Web of Science Clarivate Analytics USA and Crossref Indexed Journal*

*NAAS Journal Score 2020 (4.31)*

*Online Contents Available at: http//www.bbrc.in/*
*Doi: http://dx.doi.org/10.21786/bbrc/13.14/108*

Integrated Development Environment ease fixing design errors easily. Static RAM-based FPGA's are programmable devices and the cells store the program [2]. This program determines the functionality and routing.

Faults like latch-up and gate rupture and change in silicon structure and changes in the doping can occur in the FPGA and can lead to several defects like change in transistor behavior and timing behavior. The FPGA are generally used in space and because of the intense radiation in the space there are some challenges in using FPGA's in space. FPGA's stores data in static form radiations can harm the static memory in the FPGA. And sometimes the on-chip used sensors can also give faulty output. Hardware Redundancy is used here. The systems are used in a harsh environment so the fault tolerance and the reliability of the model should be very high. The hardware required for a TMR is thrice the hardware required for a simple system[3].

In Avionics safety is given the highest priority and for that correct readings from the sensors should be obtained and process. To improve the reliability Triple Modular Redundancy concept is used and is implemented on the modules of FPGA's. With the development of Science and Technology, the reliability of electronics has been increased in avionics. With the increase in lifetime, reprogrammability has been a stringent requirement in space development. The method by which the FPGA's store data has a high susceptibility to the single event upsets (SEUs). Single Event Transient (SET) is an event in which a current or voltage spike is induced in the circuit. The SEU results in the change in memory bits because of heavy ions, protons, and radiation ion. This contributes to the failure of the system.

SEU is the contributor to device soft failure and so the hardware will give undesired outputs [4-6]. Triple modular redundancy can be used for the hardening of the circuits implemented on SRAM-based FPGAs. LUT (Look Up Tables) are used to map the logic gates on FPGA. The interconnections are also controlled using the data which is to be stored in Static RAM. To apply the TMR on a circuit the device redundancy, system redundancy, module redundancy, and logic element redundancy need to be considered. If a fault occurs in any one of the domains TMR masks the fault by majority voting. The above method provides the correct output masked by the voter and hence makes the system resistant against SEU. TMR is a very widely used concept to improve fault tolerance. The disadvantage of the TMR is that it can handle only if one of the FPGA is not working properly. If two or three FPGA's fail simultaneously then the TMR will not work properly and give unfaithful outputs.

We can also add only the SEU sensitive gates, i.e. the gates that are prone to upset in case of SEU, in the circuits are detected using the signal probabilities of the line and are further hardened with TMR; while those non-sensitive to SEU are not hardened. Because only part of the gates is selectively hardened by TMR, so new developments can be made so that it could significantly reduce the area overhead of the hardened circuit compared to full TMR. If we want to increase the reliability of a circuit, more gates need to be hardened so the area overhead increases too; otherwise, if we want to decrease the area overhead, the number of gates to be hardened by TMR must decrease, so the reliability decreases too in the case of SEU. Therefore, a compromise between the area overhead and the number of functional errors is required. Moreover, faulty domains in the STMR system cannot be repaired [7-9].

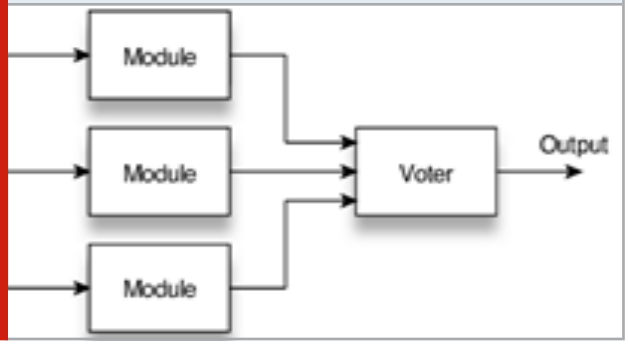
Depending on our requirement the number of functional errors and the area overhead is achieved. The Space programs are now made for a longer duration of time. So, the chances of the damage may increase and it is not possible to make any hardware changes to the FPGA's. If an FPGA is constantly giving wrong output then it can be discarded and the system can be used as a double modular redundancy.

FPGA is also used in medical applications. To give superior patient care to the pulmonary diseased diseases related to the heart the devices used in hospitals are based on the FPGA. There are many applications such as the implementation of artificial neural networks designed with help since the FPGA is a reconfigurable new pattern that can be added in the FPGA program. While using the appliances in the medical field fault tolerance and speed play a very important role. So to reduce the fault and increase the speed we use TMR and SPI communication. Our module has SPI communication between the master and the slave. This type of communication is very fast as compared to other communication protocols. Constant power is needed in the FPGA based devices and in our module, the power consumption will get tripled so it is not possible to make the devices portable with the use of FPGA. The semiconductor products continue to increase in these myriads of products.

Programmable Logic Devices have a much high adoption rate. FPGA offers a viable and powerful alternative to both ASICs especially in medical equipment development [11-13]. The utilization of PLD in this field decreases the recurring cost that is associated with ASICs. FPGA also offers design flexibility and board integration opportunities. Additionally, PLDs can be upgraded as there are changes in the field and a requirement. The cost is a bit high in FPGA but the Programmability, Speed, Flexibility are the advantages. In this, the sleep pattern of a person is monitored and then according to whether the person can have good sleep and healthy sleep. This disease is caused because the lower tongue touches the throat and snoring sound is generated. To give a complete report about that this method is used to get proper results. The inputs are fed to the sensors and sometimes there is a faulty reading so it can be eliminated. There are various sensors involved in this and all are available on the chip. The FPGA is complex and modular to deliver the required needs. To built hardware moreover, the FPGA is also enabled to store data that is obtained from the device. FPGA has a very long-life cycle and is built in such a way that has a long product cycle [14-17].

In modular Redundancy, the multiple replicates of the same modules are employed. The method to approach Correctness in a system is through an N Modular Redundancy (NMR) method. An NMR system replicates a computing source into parallel running N- module and uses voters to mask errors at the output and it is successful until the N/2 systems are concurrently at a fault. In a triple modular system, the value of N=3. As the value of N increases the reliability increases and the fault tolerance of the system increases. There are 3 inputs in the proposed system and the output of each system is feed to the input of the module called the voter. Each of the three devices executes the same particular code with the same variables and constants provided. Since the same code is given to all the systems a similar output is expected from all the N modules. The 3 modules are connected with the voter with SPI (Serial Communication Protocol) communication protocol. The triple modular redundancy system works on the principle of another majority of the values that are input to the system [15-17].

Figure 1: Block Diagram of Triple Modular Redundancy




**Mathematical Expression:** The Mathematical Expression for the Redundant system is determined by the reliability of the individual modules combined. The Equation considers that the Voter circuit does not fail. The redundant system does not fail if none of the system fails. The reliability of this system can be given by this equation where qM is the reliability of each module and (Ni) is the number of I elements subset of N elements [15-17].

$$R = \sum_{i=\frac{N}{2}}^{N} \binom{N}{i} q_M^i (1 - qM)^{N-i}$$

The reliability of the one module is denoted by Rm and the reliability of the system is denoted by R. Assuming that the failure of the three modules are mutually exclusive.

$$R=R_m^{\ 3}+3R_m^{\ 2}(1-R_m) \ ; \quad R= 3R_m^{\ 2}-2R_m^{\ 3}$$

Redundancy does not increase the reliability if the value of $R_m$ is less than 0.5 and the closer the value of $R_m$ to 1 the better is results of the system. Reliability is the probability that no failure will occur. The $R_M$ is the state where no failure will occur. The RM will produce correct output over a given span of time. The System will generate a correct output and a constant exponent function λ which defines the constant failure rate.

$R_M=e^{-\lambda t}$

Consider a simplest reliability models of a system having n modules. $R_{sys}$ is then given by

$$R_{sys}(t)=[R_M(t)]n \ ; \ R_{sys}(t)=[\ ^{e-\lambda}t]n$$

We have to note one thing that all the digital modules are independent and reliability of all modules are similar. The fault constant for all the modules I also use is similar. We also assume that the voter is working and giving faithful results. $R_I$=Probability that all the three modules are functioning + Probability that any two modules are functioning.

$$R_I=B(3:3) + B(2:3) \quad = 3R_M^{\ 2}-2R_M^{\ 3} \quad =3e-2^{t\lambda}-2e-2^{t\lambda}$$

Now we consider the reliability of voter RT.

$$R_{TMR}=R_{Voter}\ R_I; \ R_{TMR}=R_{Voter}(3e-2^{t\lambda}-2e-2^{t\lambda})$$

**Field Programming Gate Array:** Field Programming Gate Array is a programmable device that is based on CLB via programmable interconnects. FPGA and ASIC can be differentiated based on custom manufacturing for a particular task. Field Programming Gate Array is a custom configured and reliable circuit that can be programmed using Hardware Description Language. Due to programmability FPGA fit for a different market. Various manufacturers different types of FPGA board those designed especially for Wireless Communication, Aerospace, Defence, Medical Field, Image Processing, Automobile Consumer Electronics. High processing speed and control over several channels are some of the advantages. FPGA's have high data to clock rate ratio. Depending on the work and the complexity of computing and the environment to be used there are 3 types of FPGA's available and those are Low Range FPGA, Mid Range FPGA's, and High Range FPGA. A large number of Input and output will-determinism that you can achieve with an FPGA will usually far surpass that of a typical sequential processor [1-4].

In this paper, we are using Xilinx Nexyus4 Artrix 7 FPGA board. It is an application-specific integrated circuit tool. The FPGA uses an array of programmable blocks and those blocks are reconfigurable and inter-wired. Logical blocks can be configured by storing a particular response or action in the form of Look Up Tables(LUT). FPGA Logic Block also includes memory elements which are simple flip flops. The FPGA has a number of reconfigurable LUT and RAM to store and implement different complex computations at a fast rate and can communicate with the number of on built I/O ports. FPGA has a quartz crystal oscillator, an on-chip resistance oscillator, and a phase lock loop. Floor Planning is used to allocate the resources within FPGA to meet time constraints. As FPGA designs employ very fast I/O rates and bidirectional data

buses, it becomes a challenge to verify the correct timing of valid data within setup time and hold time.

One of the big disadvantages of using FPGA in space can be overcome by our module TMR. The method by which the FPGA's store data has a high susceptibility to the single event upsets (SEUs). Single Event Transient (SET) is an event in which a current or voltage spike is induced in the circuit. The SEU results in the change in memory bits because of heavy ions, protons, and radiation. This contributes to the failure of the system. SEU is the contributor to device soft failure and so the hardware will give undesired outputs. The hardening of the circuits implemented on SRAM-based FPGAs is essential. LUT(Look Up Tables) are used to map the logic gates on FPGA. The interconnections are also controlled using the data which is to be stored in Static RAM. To apply the TMR on a circuit the device redundancy, system redundancy, module redundancy, and logic element redundancy need to be considered. The above method provides the correct output masked by the voter and hence makes the system resistant against SEU. TMR is a very widely used concept to improve fault tolerance. The disadvantage of the TMR is that it can handle only if one of the FPGA is not working properly. If two or three FPGA fail simultaneously then the TMR will not work properly and give unfaithful outputs [7-10].

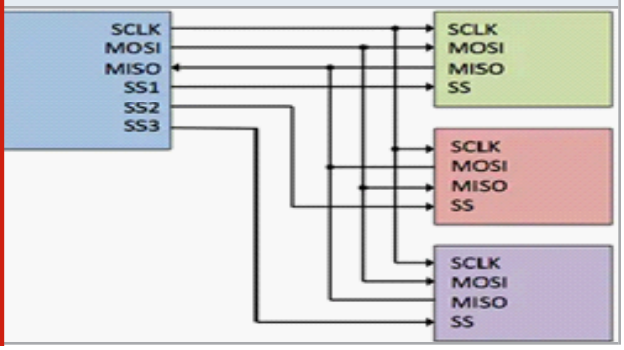
We can also add only the SEU sensitive gates, i.e. the gates that are prone to upset in case of SEU, in the circuits are detected using the signal probabilities of the line and are further hardened with TMR; while those non-sensitive to SEU are not hardened. Because only part of the gates is selectively hardened by TMR, new developments can be made so that it could significantly reduce the area overhead of the hardened circuit compared to full TMR. If we want to increase the reliability of a circuit, more gates need to be hardened so the area overhead increases too; otherwise, if we want to decrease the area overhead, the number of gates to be hardened by TMR must decrease, so the reliability decreases too in the case of SEU. In this way, the effect of radiation on FPGA can be tolerated. FPGA cannot perform the tasks such as complex rare calculations, Sorting, Searching, calculations on Floating-Point Arithmetic properly. The FPGA cannot be battery operated and especially in our case as we are using 3 slaves and master the power consumptions increase by 3 times. Also, the cost of FPGA is high.

**IV. Software:** Vivado Design Suite is a software for synthesis and analysis of HDL (Hardware Description Language) designs, with the additional system on chip development. Vivado represents a ground-up rewrite and re-thinking of the entire design flow and is a well-conceived, tightly integrated, blazing-fast, scalable, maintainable, and intuitive tool. Vivado in simulation describes the data model, integration, algorithms, and performance. Vivado enables developers to synthesize their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer. Vivado is a design environment for FPGA products from Xilinx, and is tightly-coupled to the architecture of such chips, and cannot be used with FPGA products from other vendors.

Vivado Hardware Manager is used to load the hardware designs onto the FPGAVivado's Simulator is used to simulate your design is working as expected. Integrated Logic Analyzer act as a virtual oscilloscope Vivado's High-Level Synthesis - This tool reads C based code and converts it to an HDL based design. Xilinx's Software Development Kit is the tool used to write C code that will run on the softcore processor implemented on the FPGA. Vivado is compatible with Xilinx Nexys 4 Artrix 7. General Purpose project is selected belonging to family Artrix7. The sub Family is also Artrix7. The package selected for this project is CGS324 where cgs mean Code Group Synchronization. The speed grade is -3, this speed grade is the fastest.

**V. Serial Peripheral Interface:** SPI is faster than I2C. SPI is full duplex while the I2C is half duplex. SPI has a requirement of 4 wires while the I2C has requirement of 3 wires. SPI has a single master but the I2C has multiple masters. More power consumption is there in I2C where on the other hand less power consumption is there in SPI. Both SIP and I2C are compatible with Fpga but according to our real time requirements SPI being faster and having full duplex communication we utilize SPI communication.

Figure 2: SPI master Slave




**VI. Disadvantages:** Triple Modular Redundancy with provide a fault tolerant and robust fault masking system against faults in various fields for different trade-offs between cost, reaction times, fault coverage. The disadvantage of all module level mitigation techniques is that they do not provide a simple and robust recovery mechanism after an error has been detected in one of the modules. In general logic with sequential elements, it is not ensured that the error will be detected until it is manifested on the output of the module where it is compared with the outputs of the redundant modules. The internal state of the erroneous module can at that stage be very much different from the state of the redundant modules. Any further execution will be meaning less since the erroneous state will not be automatically recovered from.

Methods like this have the disadvantage that they consume more resources, a larger space on the PCB and will dissipate additional power. Due to lower gate length technologies used in FPGAs, reliability becomes one of the major issues for mission-critical applications [1]. Though if the system is running correctly but the voter is faulty then there is no use of the system. The voter can be faulty means there are two chances either the voter is not able to take the input properly or the voter's output is faulty.

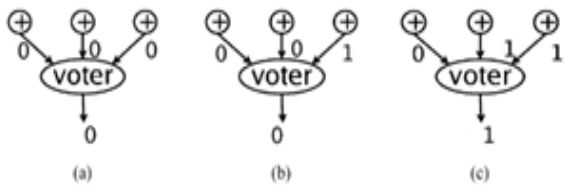
## RESULTS AND DISCUSSION

Consider the system with three modules acting as slaves and the voter acts as a master. The master initiates the communication and asks the slave to perform a particular task. The task is performed by the 3 slaves and the particular value as the output is sent to the master that is the voter. Considering the majority of the values the master (voter) gives the output. Consider three independent modules A,B and C connected with Master that is the voter with SPI communication. The following truth table represents the output of the voter with respect to the changes in the slave values.

Table 1. Truth Table of Voter Input and Output

| A | B | C | Y |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

Figure 3: (a)No fault b)Fault in 1 System with proper output (c)Fault in 2 system Improper Output




The above we see three modules that perform on the same set of inputs and give their outputs. The same code with the same inputs are provided to the inputs and the output is given to the voter. We consider that the voter is perfect and gives correct output. In figure a all the inputs are similar and the and the proper output is given by the system. In figure b the third system is not correct and it gives output other than the what the first two are offering. But due to triple Modular Redundancy the voter masks and the incorrect output and gives the correct output. Out of 3 system 2 are giving correct output and the third one is giving wrong output. Based on the input values the output value Y is determined. Y=AB+BC+AC. Figure 3(a,b,c) shows the simulated output with circuit and implementation diagram.

Table 2. Table According to Boolean Expression

| A | B | C | AB | BC | AC | Y |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Figure 3(a): Simulation

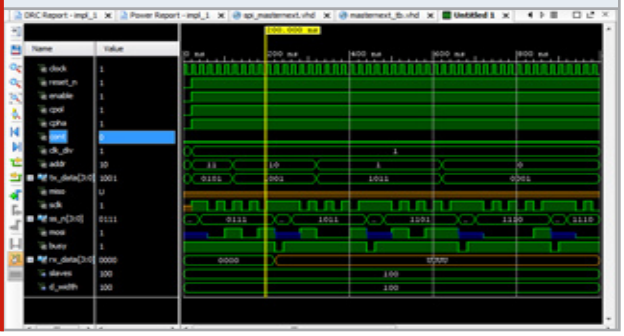


Figure 3(b): RTL schematic

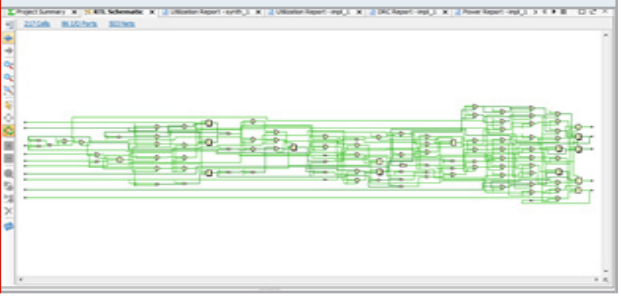
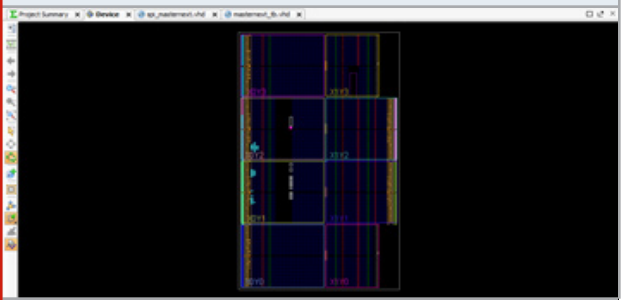


Figure 3 (c): Implementation



## CONCLUSION AND FUTURE SCOPE

Triple Modular Redundancy is a good method to mask faulty output. SPI communication provides fast communication between masters and slaves. This system can be used anywhere in which fault tolerance is required. This system can be made more fault tolerant by using a feedback path. Instead of triple modular redundancy, we can use five modular redundancy. This system can be made more robust to survive in avionics by the use of scrubbing. This system is fault tolerant, we can also make this system to correct the fault.

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